**NEPAL COLLEGE OF INFORMATION TECHNOLOGY**

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| Level: Bachelor | Assessment | Year : 2014 |
| Programme: BE ELX | | Full Marks: 100 |
| Course: Integrated Digital Electronics | | Time : 3hrs. |

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| *Candidates are required to give their answers in their own words as far as practicable.* |
| *The figures in the margin indicate full marks.* |
| Attempt all the questions. |

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|  | 1. For the BJT inverter shown below draw the voltage transfer characteristics explaining and showing the values for all the necessary points. Also find both the low and high noise margins and the logic swing. Assume βF = hfe = 50, VBE(on) = 0.65V, VBE(sat) = 0.75V, VCE(sat) = 0.2V.      1. How does I2L offer high packing density? Show the interconnection diagram for a 3 to 8 decoder in I2L and briefly explain it. | 8  7 |
| 2. | b) Shown below is an “On Chip” TTL Inverter Circuit. Use βF = 20, and βR = 0.2.   1. Sketch the VTC showing values of all the breakpoints. 2. Compute the fan-out with NMH = NML.   Untitled-1 copy | 7 |
|  | 1. Draw the circuit diagram of standard 2-input TTL NAND gate. Briefly explain input transistor action and verify its truth table. 2. Discuss the various advantages and disadvantages of ECL logic family. | 8  7 |
|  | 1. Compare various Bipolar and MOS technologies on the basis of the design parameters fan-out, power dissipation, packing density and switching speed. 2. Consider the CMOS inverter given below. Let KP=KN, |VTN| = |VTP| = 1.25 V, and VDD = 5 V. Find the transition points for the p-channel and the n-channel transistors. | 8  7 |
|  | * 1. Explain the depletion type and enhancement only N-channel MOSFET with the diagram.   b) Implement the following logic functions  using CMOS logic using NMOS logic | 8  7 |
|  | 1. Explain High Speed TTL with its application.   b) Why is the CMOS switching speed is greater than PMOS/NMOS counterparts? | 8  7 |
|  | Write short notes on (***Any Two***):   1. High Threshold Logic 2. CMOS NAND Gate 3. RTL Ex-OR Gate | 2×5 |